REMARKS

The Office Action mailed September 8, 2003, has been carefully considered. In response to the Office Action, Applicants have amended the application. Applicants request that the Examiner consider the following remarks, and then pass the application to allowance.

Art Rejection Under 35 U.S.C. § 103(a)

Claims 1-4, 7-13, 16-18 and 21-22 were rejected under 35 U.S.C. § 103(a) as unpatentable over TA (Takahashi et al., U.S. Pat. No. 6,061,283) in view of LI (Lin, U.S. Pat. No. 6,421,251), and further in view of PA (Parulkar et al., U.S. Pat. No. 6,363,509). Claims 5, 6, 15, 19 and 20 were rejected under 35 U.S.C. § 103(a) as unpatentable over TA in view of LI and PA, and further in view of MA (Matsumura et al., U.S. Pat. No. 6,370,675).

TA is directed to a method and system for generating test patterns which are used for testing an IC device which is to be fabricated. TA recognizes that accurate test patterns are necessary to ensure proper operation of a fabricated IC device, and seeks to provide these accurate test patterns in an efficient and expedient fashion. Rather than recreating these test patterns from the beginning after the device is fabricated, TA relies on the software simulation stage of the IC production process, and uses information available during the software simulation stage to create the test patterns, which can then be applied to the fabricated IC to determine proper operation.

TA is particularly concerned with ensuring that the test patterns are valid and can provide an accurate assessment of the proper operation of the IC device, and uses a suitably configured evaluation system 20 to determine the validity of the generated test pattern. While a VCD file can be used to generate and evaluate the test pattern, there is no discussion in TA of the *selection* of a simulation session range, or of a target session range within the simulation session range. Moreover, the use of the VCD file in TA is not by the operator for debugging purposes, as in the case of the presently claimed invention, but is rather for assembling and evaluating the test patterns which are to be applied to the fabricated IC. Since the test patterns are intended as a global tool for testing of the operation of the IC in virtually all conditions and with all combinations of inputs, there would be no value to selectively targeting ranges, and ranges within ranges, or to generating a VCD file "dedicated to the state information in the selected simulation target range and being exclusive of state information outside said selected simulation target range," as is presently claimed. TA neither contemplates this type of approach, nor has any use for it.

Further, none of LI, PA or MA remedies this shortcoming. LI in particular, in the Post-Simulation Analysis Mode section in cols. 41 and 42, discusses logging frequency in support of VCD, but only mentions that this frequency can be adjusted. There is no discussion of selection of simulation ranges, or target ranges, or of generating VCD files "dedicated to the state information in the selected simulation target range and being exclusive of state information outside said selected simulation target range." Accordingly, considered singularly or combination, TA fails to render obvious the teachings of the present invention, and withdrawal of the obviousness rejection based on same is respectfully requested.

Conclusion

In view of the preceding discussion, Applicants respectfully urge that the claims of the present application define patentable subject matter and should be passed to allowance. Such allowance is respectfully solicited.

If the Examiner believes that a telephone call would help advance prosecution of the present invention, the Examiner is kindly invited to call the undersigned attorney.

Respectfully submitted,

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